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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,370	04/09/2004	Anders Landin	5181-99901	1207
58467	7590	11/16/2007		
MHKKG/SUN			EXAMINER	
P.O. BOX 398			ELAND, SHAWN	
AUSTIN, TX 78767				
			ART UNIT	PAPER NUMBER
			2188	
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			11/16/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/821,370		LANDIN ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Shawn Eland		2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 October 2007.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-17 and 19-48 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-17 and 19-48 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/28/07 has been entered.

### ***Status of Claims***

Claims 1, 3 – 17, & 19 – 48 are pending in the Application.

Claims 1, 4 – 14, 16 – 17, 20 – 30, 32 – 34, 36 – 46, & 48 have been amended.

Claims 2 & 18 are cancelled.

Claims 1, 3 – 17, & 19 – 48 are rejected.

### ***Response to Arguments***

Applicant's arguments filed 09/28/07 have been fully considered but they are not persuasive.

The Examiner fails to see how the kind of memory used matters in this regard. If the cache memory of Liencres performs the same functions as the system memory in Applicant's invention, would that not also mean that the Liencres memory could also be considered system memory? Due to the memory's functions, there is no appreciable difference between the two memories and therefore the Examiner considers them to be one and the same for this application.

Memory simply stores data. In order to get the data there must be some kind of controller or manager that knows what to get and send the data out. The data is sent from the memory to the active device via this controller. This is how the Examiner interpreted the claim language for system memory sending data or a report.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 – 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Liencre*** (5,434,993) in view of ***Chandrasekaran*** (US 6,970,872) and ***Roy*** (US 6,065,092).

In regard to claim 1, Liencre teaches a node (*see element 20*) including an active device (*see element 21*), an interface to an inter-node network (*see element 31*), a memory (*see element 37*), and an address network coupling the active device, the interface, and the memory (*see element 33*); an additional node coupled to the node by the inter-node network (*see figure 3a; see column 6, lines 11 - 15*); wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the memory is configured to send data corresponding to the coherency unit to the active device dependent on memory response information associated with the coherency unit (*see column 7, "Read*

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*Transactions*”), wherein the memory response information includes information used to derive global access state information for the coherency unit (*col. 1, lines 64 – 65*).

In regard to claim 17, Liencres teaches a plurality of devices including a memory (*see element 37*), an active device (*see element 21*), and an interface to an inter-node network coupling nodes in the multi-node computer system (*see element 31*); an address network configured to convey packets between the plurality of devices (*see element 33*); wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the memory is configured to send data corresponding to the coherency unit to the active device dependent on memory response information associated with the coherency unit (*see column 7, “Read Transactions”*), wherein the memory response information includes information used to derive global access state information for the coherency unit (*col. 1, lines 64 – 65*).

In regard to claim 33, Liencres teaches an active device (*see element 21*) included in the node initiating a transaction to gain an access right to a coherency unit by sending an address packet on an address network included in the node (*see column 7, “Read Transactions”*); dependent on memory response information associated with the coherency unit, a memory included in the node sending data corresponding to the coherency unit to the active device in response to the address packet (*see column 7, “Read Transactions”; if the node owns the coherency unit, there is no need to look for the data on other nodes*), wherein the memory response information includes information used to derive global access state information for the coherency unit (*col. 1, lines 64 – 65*).

In regard to claims 1, 17, & 33, Liencres does not teach wherein if the transaction cannot be satisfied within the node, the memory is configured to forward a report corresponding to the address packet to the interface, wherein in response to the report, the interface is configured to send a coherency message requesting the access right to another one of the nodes via the inter-node network.

However, Chandrasekaran teaches a multi-node network (*figure 1*) that employs several techniques to reduce latency. One of the methods employed is “write-time” validity checking (*col. 6, lines 25 – 36*). When another node writes out data, it sends out a report stating the latest write time for that data. The read data is invalid once its timestamp comes before the latest write time. The node, now having an invalid read data, will now have to request the updated data from the additional node. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ optimistic reading of data using “write-time” validity checking so that reads could be employed when another node has exclusive access but hasn’t yet written the data.

Also in regard to claims 1, 17, & 33 Liencres does not teach wherein the node has a data network that is separate from the address network. However, it is well known in the art to have separate data and address networks, as cited in Roy (*col. 3, lines 61 – 67 through col. 4, lines 1 – 5*). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Liencres’s invention by separating the network into separate address and data networks in order to improve performance using interleaving.

For claim 34, Liencres teaches wherein said forwarding the report comprises the system memory send a data packet including the report to the interface via a data network included in the node (*see element 33*).

For claims 3, 19, & 35, Lawrence teaches wherein the memory response information is configured to identify one of at least two possible response states (*see column 7, "Read Transactions", last sentence; see column 1, lines 64 - 65*).

For claims 4, 20, & 36, Liencres teaches wherein if the memory response information indicates a no response state, the system memory is configured to send neither the data nor the report in response to the address packet; wherein when the memory response information indicates the no response state, an additional active device (*see element 35*) included in the node has an ownership responsibility for the coherency unit and is configured to supply the data to the active device in response to receiving the address packet (*see column 7, "Read Transactions"*).

For claims 5 & 21, Liencres teaches wherein if the address packet is conveyed in point-to-point mode by the address network (*see element 33 in figure 3a; having only 2 processors would, in effect, be a point-to-point mode*), the system memory is configured to send an additional address packet indicating the transaction to the additional active device having the ownership responsibility for the coherency unit (*see column 7, "Read Transactions", 1<sup>st</sup> paragraph; the processor cache memory 37 indicates to the processor cache controller 35 that the memory request cannot be fulfilled*).

For claim 37, Liencres teaches the system memory sending an additional address packet indicating the transaction to the additional active device having the ownership responsibility for the coherency unit (*see column 7, "Read Transactions", 1<sup>st</sup> paragraph; the processor cache*

*memory 37 indicates to the processor cache controller 35 that the memory request cannot be fulfilled) if the address packet is conveyed in point-to-point mode by the address network (see element 33 in figure 3a; having only 2 processors would, in effect, be a point-to-point mode).*

For claims 6 & 22, Liencres teaches wherein the system memory is configured to update the memory response information to indicate the no response state in response to receiving the address packet, and wherein the active device is configured to gain an ownership responsibility for the address packet in response to receiving the address packet *(see figure 1c; if there's no response, then the processor will take the data from main memory and subsequently "own" it until it does a write-back).*

For claim 38, Liencres teaches the system memory updating the memory response information to indicate the no response state in response to receiving the address packet; and the active device gaining an ownership responsibility for the address packet in response to receiving the address packet *(see figure 1c; if there's no response, then the processor will take the data from main memory and subsequently "own" it until it does a write-back).*

For claims 7 & 23, Liencres teaches wherein the system memory is configured to update the memory response information to indicate a response state in response to receiving an address packet providing the system memory with an ownership responsibility for the coherency unit; wherein if the memory response information identifies the response state, the system memory is configured to send the data corresponding to the coherency unit to the active device in response to the address packet *(see column 7, "Read Transactions"; see figure 1c; if the data does not exist in cache, it will be owned by the node).*



For claim 39, Liencres teaches the system memory updating the memory response information to indicate a response state in response to receiving an address packet providing the system memory with an ownership responsibility for the coherency unit; wherein if the memory response information identifies the response state, the memory sends the data corresponding to the coherency unit to the active device in response to the address packet (*see column 7, "Read Transactions"; see figure 1c; if the data does not exist in cache, it will be owned by the node*).

For claims 8, 24, & 40, Liencres teaches wherein if the memory response information indicates a shared response state, the system memory is configured to not send the report and to send the data corresponding to the coherency unit if the access right is a read access right (*see column 7, "Read Transactions"*); wherein if the memory response information indicates the shared response state and the access right is a write access right, the system memory is configured to not send the data to the active device and to send the report to the interface (*see column 7, "Write Transaction"*).

For claims 9, 25, & 41, Liencres teaches wherein the system memory is configured to update the response information to indicate the shared response state in response to a proxy address packet sent by the interface indicating that an additional active device in the additional node is requesting read access to the coherency unit (*see column 7, "Read Transactions"; according to [00189] in the applicant's specification, proxy packets are packets sent by the interface 148; the processor cache controller 35 and the interface 148 are one and the same*).

For claims 10, 26, & 42, Liencres teaches wherein if the memory response information indicates an invalid response state, the system memory is configured to not send the data to the

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active device and to send the report to the interface in response to the address packet (*see column 7, "Read Transactions"; see column 1, lines 64 - 67*).

For claims 11, 27, & 43, Liencres teaches wherein the system memory is configured to update the memory response information to indicate the invalid response state in response to receiving a proxy address packet from the interface indicating that an additional active device included in the additional node is requesting write access to the coherency unit (*see column 1, lines 64 - 68 through column 2, lines 1 - 4*).

For claims 12, 28, & 44, Liencres teaches wherein the system memory is configured to send the data dependent on both the memory response information and a global access state of the coherency unit within the node, wherein the memory is configured to send the report dependent on the global access state (*see column 7, "Read Transactions"; see column 1, lines 64 - 68 through column 2, lines 1 - 12*).

For claims 13, 29, & 45, Liencres teaches wherein the system memory is configured to include a value of the memory response information in the report, wherein the value is a value of the memory response information before the memory response information is modified in response to the address packet (*see column 1, lines 64 - 65*).

For claims 14 & 30, Liencres teaches wherein the interface is configured to maintain a plurality of records in an outstanding transaction queue, wherein each of the plurality of records corresponds to a respective report received from the system memory, and wherein the interface is configured to determine a global access state of the coherency unit in the node from the value of the memory response information included in the report and from one or more of the records in the outstanding transaction queue (*see element 40; see column 9, lines 32 - 47*).

For claim 46, Liencres teaches the interface maintaining a plurality of records in an outstanding transaction queue, wherein each of the plurality of records corresponds to a respective report received from the system memory; and the interface determining a global access state of the coherency unit in the node from the value of the memory response information included in the report and from one or more of the records in the outstanding transaction queue *(see element 40; see column 9, lines 32 – 47)*.

For claim 15, Liencres teaches in response to receiving an additional coherency message specifying the coherency unit from the additional node, the interface is configured to select a type of proxy address packet to send on the address network dependent on the global access state *(see column 8, lines 56 – 62)*.

For claim 31, Liencres teaches in response to receiving an additional coherency message specifying the coherency unit from another node, the interface is configured to select a type of proxy address packet to send on the address network dependent on the global access state *(see column 8, lines 56 – 62)*.

For claim 47, Liencres teaches in response to receiving an additional coherency message specifying the coherency unit from the additional node, the interface selecting a type of proxy address packet to send on the address network dependent on the global access state *(see column 8, lines 56 – 62)*.

For claims 16 & 32, Liencres teaches if the system memory subsequently updates the memory response information again in response to another address packet, the system memory is configured to provide a new value of the memory response information to the interface *(see column 9, lines 1 – 8)*.

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For claim 48, Liencres teaches if the system memory subsequently updates the memory response information again in response to another address packet, the system memory providing a new value of the memory response information to the interface (*see column 9, lines 1 – 8*).

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*Examiner's Information*

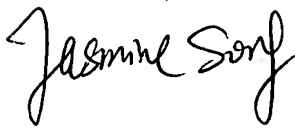

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on MO - TH, & every other FR.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Shawn Eland  
11/13/2007

Primary Examiner